PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
E876-PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/JP 97/ 02987	27/08/1997	27/08/1996
Applicant		
NIPPON STEEL CORPORATION et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. [ ] **Certain claims were found unsearchable** (see Box I).

2. [ ] **Unity of invention is lacking** (see Box II).

3. [ ] The international application contains disclosure of a **nucleotide and/or amino acid sequence listing** and the international search was carried out on the basis of the sequence listing
   - [ ] filed with the international application.
   - [ ] furnished by the applicant separately from the international application,
     - [ ] but not accompanied by a statement to the effect that it did not include matter going beyond the disclosure in the international application as filed.
   - [ ] Transcribed by this Authority

4. With regard to the **title,**
   - [X] the text is approved as submitted by the applicant
   - [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   - [ ] the text is approved as submitted by the applicant
   - [X] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this International Search Report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is:
   Figure No. 2
   - [X] as suggested by the applicant.
   - [ ] because the applicant failed to suggest a figure.
   - [ ] because this figure better characterizes the invention.
   - [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP 97/02987

Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)

A semiconductor device (1) comprising electrodes formed on a semiconductor chip (2) and bumps (3) which consist of a low melting point metall ball spherically formed and having a given size and which are adhesive bonded to the electrodes (5). The electrodes (5) are formed from an electrode material of Cu or a Cu alloy, Al or an Al alloy, or Au or a Au alloy. When the electrode material is composed of Al or an Al alloy, the electrodes contain, on the electrode material layer of Al or an Al alloy, at least one layer (6) composed of a metal or metal alloy (preferably a metal selected form Ti, W, Ni, Cr, Au, Pd, Cu, Pt, Ag, Sn or Pb, or an alloy of these metals) having a melting point higher than the electrode material. The low melting point metal balls (3) are adhesive bonded to the electrodes (5) preferably with a flux. The low melting point metal balls (3) adhesive bonded to the respective electrodes (3) may also be reflowed to form semispherical bumps (10) before use.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 97/02987

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/485

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	PATENT ABSTRACTS OF JAPAN vol. 097, no. 007, 31 July 1997 & JP 09 082719 A (NIPPON STEEL CORP), 28 March 1997, see the whole document ---	1,2,7,8, 10-12, 14,15
X	PATENT ABSTRACTS OF JAPAN vol. 095, no. 003, 28 April 1995 & JP 06 333930 A (OKI ELECTRIC IND CO LTD), 2 December 1994, see the whole document ---	1,2,7,8, 10-12, 14,15
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 082 (E-1038), 26 February 1991 & JP 02 299288 A (FUJITSU LTD), 11 December 1990, see the whole document ---	1,2,7,8, 10,11, 14,15

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 January 1998	23/01/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Zeisler, P

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 096, no. 009, 30 September 1996 & JP 08 118005 A (MATSUSHITA ELECTRIC IND CO LTD), 14 May 1996,	1,2,7,8, 10,11, 14,15
Y	see the whole document & US 5 655 704 A (MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.) 12 August 1997 see column 6, line 16 - line 43; figure 4	9,13
A	PATENT ABSTRACTS OF JAPAN vol. 008, no. 281 (E-286), 21 December 1984 & JP 59 148352 A (SEIKO DENSHI KOGYO KK), 25 August 1984, see the whole document	1-7,10, 11
A	US 5 219 117 A (LIN PAUL T) 15 June 1993 see the whole document	1,3-7, 10,14,15
Y	EP 0 527 387 A (NIPPON STEEL CORP) 17 February 1993 see column 9, line 38 - column 10, line 4; figures 3A,3B	9,13
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 275 (E-1219), 19 June 1992 & JP 04 065130 A (FUJITSU LTD), 2 March 1992, see abstract	9,13
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 046 (E-1029), 4 February 1991 & JP 02 278831 A (FUJITSU LTD), 15 November 1990, see abstract	9,13

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 97/02987

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5219117 A	15-06-93	NONE	
EP 0527387 A	17-02-93	JP 3097237 A	23-04-91
		JP 3097240 A	23-04-91
		DE 69027448 D	18-07-96
		DE 69027448 T	10-10-96
		EP 0427384 A	15-05-91
		KR 9404246 B	19-05-94
		US 5164336 A	17-11-92
		US 5114878 A	19-05-92
		JP 1995827 C	08-12-95
		JP 3174737 A	29-07-91
		JP 7019800 B	06-03-95

PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No.

International Filing Date

PCT 27. 8. 97 受領印

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference *(if desired) (12 characters maximum)* E876-PCT

Box No. I TITLE OF INVENTION

SEMICONDUCTOR DEVICE PROVIDED WITH LOW MELTING POINT METAL BUMPS AND PROCESS FOR PRODUCING SAME

Box No. II APPLICANT

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

NIPPON STEEL CORPORATION

6-3, Otemachi 2-chome, Chiyoda-ku, TOKYO 100-71 JAPAN

☐ This person is also inventor.

Telephone No.

Facsimile No.

Teleprinter No.

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of: ☐ all designated States ☑ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

TATSUMI Kohei

C/O NIPPON STEEL CORPORATION Technical Development Bureau

35-1, Ida 3-chome, Nakahara-ku, Kawasaki City, KANAGAWA 211 JAPAN

This person is:

☐ applicant only

☑ applicant and inventor

☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☑ the United States of America only ☐ the States indicated in the Supplemental Box

☑ Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: ☑ agent ☐ common representative

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

Patent Attorney (7751) ISHIDA Takashi

A. AOKI & ASSOCIATES
Toranomon 37 Mori Bldg., 5-1, Toranomon 3-chome,

Minato-ku, TOKYO 105 JAPAN

Telephone No. 03-5470-1900

Facsimile No. 03-5470-1911

Teleprinter No. J 26282

☐ Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

EL303285061US

Continuation of Box No. III FURTHER APPLICANTS AND/OR (FURTHER) INVENTORS

If none of the following sub-boxes is used, this sheet is not to be included in the request.

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

SHIMOKAWA Kenji

C/O NIPPON STEEL CORPORATION Technical Development Bureau

35-1, Ida 3-chome, Nakahara-ku, Kawasaki City, KANAGAWA 211 JAPAN

This person is:
- ☐ applicant only
- ☑ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☑ the United States of America only
- ☐ the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

HASHINO Eiji

C/O NIPPON STEEL CORPORATION Technical Development Bureau

35-1, Ida 3-chome, Nakahara-ku, Kawasaki City, KANAGAWA 211 JAPAN

This person is:
- ☐ applicant only
- ☑ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☑ the United States of America only
- ☐ the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

This person is:
- ☐ applicant only
- ☐ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality:

State *(i.e. country)* of residence:

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☐ the United States of America only
- ☐ the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

This person is:
- ☐ applicant only
- ☐ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality:

State *(i.e. country)* of residence:

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☐ the United States of America only
- ☐ the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on another continuation sheet.

Box No.V DESIGNATION OF STATES

The following designations are hereby made under Rule 4.9(a) *(mark the applicable check-boxes; at least one must be marked)*:

Regional Patent

- ☐ AP ARIPO Patent: GH Ghana, KE Kenya, LS Lesotho, MW Malawi, SD Sudan, SZ Swaziland, UG Uganda, ZW Zimbabwe, and any other State which is a Contracting State of the Harare Protocol and of the PCT
- ☐ EA Eurasian Patent: AM Armenia, AZ Azerbaijan, BY Belarus, KG Kyrgyzstan, KZ Kazakstan, MD Republic of Moldova, RU Russian Federation, TJ Tajikistan, TM Turkmenistan, and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT
- ☑ EP European Patent: AT Austria, BE Belgium, CH and LI Switzerland and Liechtenstein, DE Germany, DK Denmark, ES Spain, FI Finland, FR France, GB United Kingdom, GR Greece, IE Ireland, IT Italy, LU Luxembourg, MC Monaco, NL Netherlands, PT Portugal, SE Sweden, and any other State which is a Contracting State of the European Patent Convention and of the PCT
- ☐ OA OAPI Patent: BF Burkina Faso, BJ Benin, CF Central African Republic, CG Congo, CI Côte d'Ivoire, CM Cameroon, GA Gabon, GN Guinea, ML Mali, MR Mauritania, NE Niger, SN Senegal, TD Chad, TG Togo, and any other State which is a member State of OAPI and a Contracting State of the PCT *(if other kind of protection or treatment desired, specify on dotted line)* .....

National Patent *(if other kind of protection or treatment desired, specify on dotted line)*:

- ☐ AL Albania .....
- ☐ AM Armenia .....
- ☐ AT Austria .....
- ☐ AU Australia .....
- ☐ AZ Azerbaijan
- ☐ BA Bosnia and Herzegovina .....
- ☐ BB Barbados
- ☐ BG Bulgaria .....
- ☐ BR Brazil .....
- ☐ BY Belarus
- ☐ CA Canada
- ☐ CH and LI Switzerland and Liechtenstein
- ☑ CN China .....
- ☐ CU Cuba .....
- ☐ CZ Czech Republic .....
- ☐ DE Germany .....
- ☐ DK Denmark .....
- ☐ EE Estonia .....
- ☐ ES Spain .....
- ☐ FI Finland .....
- ☐ GB United Kingdom
- ☐ GE Georgia .....
- ☐ GH Ghana .....
- ☐ HU Hungary .....
- ☐ IL Israel .....
- ☐ IS Iceland
- ☑ JP Japan .....
- ☐ KE Kenya .....
- ☐ KG Kyrgyzstan .....
- ☐ KP Democratic People's Republic of Korea .....
- ☑ KR Republic of Korea .....
- ☐ KZ Kazakstan .....
- ☐ LC Saint Lucia
- ☐ LK Sri Lanka
- ☐ LR Liberia
- ☐ LS Lesotho .....
- ☐ LT Lithuania
- ☐ LU Luxembourg .....
- ☐ LV Latvia
- ☐ MD Republic of Moldova .....
- ☐ MG Madagascar .....
- ☐ MK The former Yugoslav Republic of Macedonia .....
- ☐ MN Mongolia
- ☐ MW Malawi .....
- ☐ MX Mexico .....
- ☐ NO Norway
- ☐ NZ New Zealand .....
- ☐ PL Poland .....
- ☐ PT Portugal .....
- ☐ RO Romania
- ☐ RU Russian Federation .....
- ☐ SD Sudan
- ☐ SE Sweden
- ☑ SG Singapore
- ☐ SI Slovenia .....
- ☐ SK Slovakia .....
- ☐ SL Sierra Leone
- ☐ TJ Tajikistan .....
- ☐ TM Turkmenistan .....
- ☐ TR Turkey .....
- ☐ TT Trinidad and Tobago .....
- ☐ UA Ukraine .....
- ☐ UG Uganda .....
- ☑ US United States of America .....
- ☐ UZ Uzbekistan .....
- ☐ VN Viet Nam .....
- ☐ YU Yugoslavia .....
- ☐ ZW Zimbabwe

Check-boxes reserved for designating States (for the purposes of a national patent) which have become party to the PCT after issuance of this sheet:

- ☐ .....
- ☐ .....
- ☐ .....
- ☐ .....
- ☐ .....

In addition to the designations made above, the applicant also makes under Rule 4.9(b) all designations which would be permitted under the PCT except the designation(s) of _____.

The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. *(Confirmation of a designation consists of the filing of a notice specifying that designation and the payment of the designation and confirmation fees. Confirmation must reach the receiving Office within the 15-month time limit.)*

See Notes to the request form

Supplemental Box *If the Supplemental Box is not used, this sheet need not be included in the request.*

Use this box in the following cases:

1. If, in any of the Boxes, the space is insufficient to furnish all the information:	*in such case, write "Continuation of Box No. ..." [indicate the number of the Box] and furnish the information in the same manner as required according to the captions of the Box in which the space was insufficient;*
in particular:	
(i) if more than two persons are involved as applicants and/or inventors and no "continuation sheet" is available:	*in such case, write "Continuation of Box No. III" and indicate for each additional person the same type of information as required in Box No. III. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below;*
(ii) if, in Box No. II or in any of the sub-boxes of Box No. III, the indication "the States indicated in the Supplemental Box" is checked:	*in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the applicant(s) involved and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is applicant;*
(iii) if, in Box No. II or in any of the sub-boxes of Box No. III, the inventor or the inventor/applicant is not inventor for the purposes of all designated States or for the purposes of the United States of America:	*in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the inventor(s) and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is inventor;*
(iv) if, in addition to the agent(s) indicated in Box No. IV, there are further agents:	*in such case, write "Continuation of Box No. IV" and indicate for each further agent the same type of information as required in Box No. IV;*
(v) if, in Box No. V, the name of any State (or OAPI) is accompanied by the indication "patent of addition," or "certificate of addition," or if, in Box No. V, the name of the United States of America is accompanied by an indication "Continuation" or "Continuation-in-part":	*in such case, write "Continuation of Box No. V" and the name of each State involved (or OAPI), and after the name of each such State (or OAPI), the number of the parent title or parent application and the date of grant of the parent title or filing of the parent application;*
(vi) if there are more than three earlier applications whose priority is claimed:	*in such case, write "Continuation of Box No. VI" and indicate for each additional earlier application the same type of information as required in Box No. VI.*
2. If the applicant claims, in respect of any designated Office, the benefits of provisions of the national law concerning non-prejudicial disclosures or exceptions to lack of novelty:	*in such case, write "Statement Concerning Non-Prejudicial Disclosures or Exceptions to Lack of Novelty" and furnish that statement below.*

Continuation of Box No. IV

Name : Patent Attorney (8627) YOSHIDA Tsuguo

Name : Patent Attorney (8826) TODA Toshio

Name : Patent Attorney (8289) NISHIYAMA Masaya

Address: Same as the address mentioned in Box No. IV

Box No. VI PRIORITY CLAIM Further priority claims are indicated in the Supplemental Box ☐

The priority of the following earlier application(s) is hereby claimed:

Country *(in which, or for which, the application was filed)*	Filing Date *(day/month/year)*	Application No.	Office of filing *(only for regional or international application)*
item (1) JAPAN	27. 08. 96	Patent Application 8 −244269	
item (2)			
item (3)			

Mark the following check-box if the certified copy of the earlier application is to be issued by the Office which for the purposes of the present international application is the receiving Office (a fee may be required):

☐ The receiving Office is hereby requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) identified above as item(s) : _____

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(If two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used):* ISA / EP

Earlier search *Fill in where a search (international, international-type or other) by the International Searching Authority has already been carried out or requested and the Authority is now requested to base the international search, to the extent possible, on the results of that earlier search. Identify such search or request either by reference to the relevant application (or the translation thereof) or by reference to the search request:*

Country (or regional Office): Date *(day/month/year)*: Number:

Box No. VIII CHECK LIST

This international application contains the following number of sheets:

1. request	:	5 sheets
2. description	:	12 sheets
3. claims	:	3 sheets
4. abstract	:	1 sheets
5. drawings	:	4 sheets
Total	:	25 sheets

This international application is accompanied by the item(s) marked below:

1. ☐ separate signed power of attorney
2. ☐ copy of general power of attorney
3. ☐ statement explaining lack of signature
4. ☐ priority document(s) *identified in Box No. VI as item(s):*
5. ☑ fee calculation sheet
6. ☐ separate indications concerning deposited microorganisms
7. ☐ nucleotide and/or amino acid sequence listing (diskette)
8. ☐ other *(specify)*:

Figure No. 2 of the drawings (if any) should accompany the abstract when it is published.

Box No. IX SIGNATURE OF APPLICANT OR AGENT

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request).

Takashi Ishida
ISHIDA Takashi

Toshio Toda
TODA Toshio

Tsuguo Yoshida
YOSHIDA Tsuguo

M. Nishiyama
NISHIYAMA Masaya

For receiving Office use only

1. Date of actual receipt of the purported international application:
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:
4. Date of timely receipt of the required corrections under PCT Article 11(2):
5. International Searching Authority specified by the applicant: ISA /
6. ☐ Transmittal of search copy delayed until search fee is paid

2. Drawings:
☐ received:
☐ not received:

For International Bureau use only

Date of receipt of the record copy by the International Bureau:

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 23/485

A1

(11) International Publication Number: WO 98/09332

(43) International Publication Date: 5 March 1998 (05.03.98)

(21) International Application Number: PCT/JP97/02987

(22) International Filing Date: 27 August 1997 (27.08.97)

(30) Priority Data:
8/244269 27 August 1996 (27.08.96) JP

(71) Applicant *(for all designated States except US)*: NIPPON STEEL CORPORATION [JP/JP]; 6-3, Otemachi 2-chome, Chiyoda-ku, Tokyo 100-71 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: TATSUMI, Kohei [JP/JP]; Nippon Steel Corporation Technical Development Bureau, 35-1, Ida 3-chome, Nakahara-ku, Kawasaki City, Kanagawa 211 (JP). SHIMOKAWA, Kenji [JP/JP]; Nippon Steel Corporation Technical Development Bureau, 35-1, Ida 3-chome, Nakahara-ku, Kawasaki City, Kanagawa 211 (JP). HASHINO, Eiji [JP/JP]; Nippon Steel Corporation Technical Development Bureau, 35-1, Ida 3-chome, Nakahara-ku, Kawasaki City, Kanagawa 211 (JP).

(74) Agents: ISHIDA, Takashi et al.; A. Aoki & Associates, Toranomon 37 Mori Building, 5-1, Toranomon 3-chome, Minato-ku, Tokyo 105 (JP).

(81) Designated States: CN, JP, KR, SG, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published

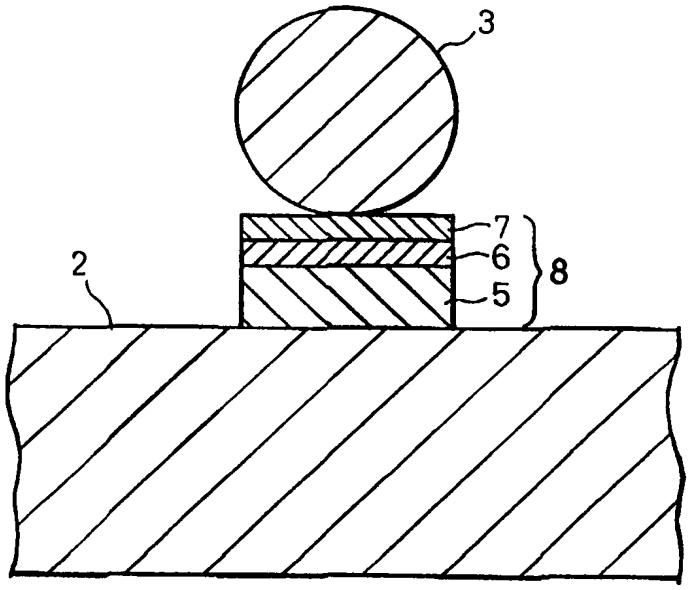
With international search report.

Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: SEMICONDUCTOR DEVICE PROVIDED WITH LOW MELTING POINT METAL BUMPS AND PROCESS FOR PRODUCING SAME

(57) Abstract

A semiconductor device (1) comprising electrodes formed on a semiconductor chip (2) and bumps (3) which consist of a low melting point metal ball spherically formed and having a given size and which are adhesive bonded to the electrodes (5). The electrodes (5) are formed from an electrode material of Cu or a Cu alloy, Al or an Al alloy, or Au or a Au alloy. When the electrode material is composed of Al or an Al alloy, the electrodes contain, on the electrode material layer of Al or an Al alloy, at least one layer (6) composed of a metal or metal alloy (preferably a metal selected from Ti, W, Ni, Cr, Au, Pd, Cu, Pt, Ag, Sn or Pb, or an alloy of these metals) having a melting point higher than the electrode material. The low melting point metal balls (3) are adhesive bonded to the electrodes (5) preferably with a flux. The low melting point metal balls (3) adhesive bonded to the respective electrodes (3) may also be reflowed to form semispherical bumps (10) before use.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania
AM	Armenia
AT	Austria
AU	Australia
AZ	Azerbaijan
BA	Bosnia and Herzegovina
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CU	Cuba
CZ	Czech Republic
DE	Germany
DK	Denmark
EE	Estonia
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GE	Georgia
GH	Ghana
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IL	Israel
IS	Iceland
IT	Italy
JP	Japan
KE	Kenya
KG	Kyrgyzstan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakstan
LC	Saint Lucia
LI	Liechtenstein
LK	Sri Lanka
LR	Liberia
LS	Lesotho
LT	Lithuania
LU	Luxembourg
LV	Latvia
MC	Monaco
MD	Republic of Moldova
MG	Madagascar
MK	The former Yugoslav Republic of Macedonia
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
MX	Mexico
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SG	Singapore
SI	Slovenia
SK	Slovakia
SN	Senegal
SZ	Swaziland
TD	Chad
TG	Togo
TJ	Tajikistan
TM	Turkmenistan
TR	Turkey
TT	Trinidad and Tobago
UA	Ukraine
UG	Uganda
US	United States of America
UZ	Uzbekistan
VN	Viet Nam
YU	Yugoslavia
ZW	Zimbabwe

DESCRIPTION

SEMICONDUCTOR DEVICE PROVIDED WITH LOW MELTING POINT METAL BUMPS AND PROCESS FOR PRODUCING SAME

Technical Field

The present invention relates to a semiconductor device provided with low melting point metal bumps and a process for producing the same.

Background Art

Semiconductor devices have currently been used widely in various fields. The semiconductor devices are usually used by mounting them on substrates. The mounting methods include bonding methods such as tape automated bonding (TAB), wire bonding and flip chip bonding.

The TAB and wire bonding are technologies by which a semiconductor device is mounted on a substrate through leads. The leads are arranged in one row per peripheral side of the semiconductor device. The technologies are, therefore, not suited to high density mounting of the semiconductor devices. In contrast to the technologies mentioned above, flip chip bonding is a technology by which the electrodes of a semiconductor device are directly connected to the electrode terminals on the substrate through a bonding metal. Since the electrodes of the semiconductor device can be provided in a lattice-like form on the entire surface, the technology is suited to high density mounting. Various solders are generally used as bonding metal in flip chip bonding because the bonding is conducted by melting at low temperature.

In flip chip bonding, semiconductor devices provided with low melting point metal bumps for bonding placed on electrodes are used, and the semiconductor devices are connected to the electrode terminals of substrates by a reflowing procedure by which the bumps are melted and solidified again.

In general, the bumps are formed by vapor deposition or plating. However, such bump formation methods must all repeat complicated treatments steps using a mask. Moreover, in the method of forming the bumps by vapor deposition, a bump material is deposited on portions where the bumps are not to be formed, and the deposition amount thereon is very large. The method is, therefore, not a preferred one in view of the cost and efficiency. Moreover, wet plating such as electroplating or electroless plating fouls wafers and causes an environmental problem, and countermeasures against such problems are indispensable. As illustrated above, conventional methods for forming the bumps are relatively costly, and practical use of the methods is restricted.

There is a stud bump procedure as a method for forming bumps other than vapor deposition and plating. Since bumps are formed one by one in the procedure, the production efficiency is low, and in addition the bump amount tends to vary among the bumps. Accordingly, securing uniformity in bonding the semiconductor devices and the substrates is difficult.

Disclosure of the Invention

An object of the present invention is to provide a semiconductor device provided with low melting point metal bumps of high quality and capable of being mounted on a substrate by flip chip bonding, and a process for producing the same.

The semiconductor device of the present invention comprises electrodes formed on a semiconductor chip, and is provided with bumps each consisting of a low melting point metal ball which is spherically formed and has a given size, and adhesive bonded to the electrodes.

The low melting point metal balls are preferably adhesive bonded to the respective electrodes with a flux.

The electrodes on the semiconductor chip are preferably formed from an electrode material of Cu or a Cu alloy, Al or an Al alloy, or Au or a Au alloy.

When the electrode material is Al or an Al alloy, at least one layer of a metal or a metal alloy having a melting point higher than the electrode material is preferably laminated to the layer formed from the electrode material.

The laminated layers are preferably formed from a metal selected from Ti, W, Ni, Cr, Au, Pd, Cu, Pt, Ag, Sn and Pb, or an alloy of these metals.

It is preferred that, of the layers laminated to the electrode material layer, the layer contacted with the electrode material layer be formed from Ti, W, Ni, Cr, Pd, Cu or Pt, or an alloy of these metals, and that the layer contacted with the low melting point metal ball be formed from Ni, Au, Pd, Cu, Pt, Ag, Sn or Pb, or an alloy of these metals.

The process for producing a semiconductor device according to the present invention is a process for producing a semiconductor device having electrodes formed on a semiconductor chip, and provided with bumps which consist of low melting point metal balls each being formed spherically and having a given size, and which are adhesive bonded to the respective electrodes, and is characterized by the low melting point metal balls being adhesive bonded and fixed to the respective electrodes with a flux.

The flux is preferably applied to the electrodes.

On another aspect of the present invention, the process for producing a semiconductor device according to the present invention is a process for producing a semiconductor device provided with low melting point metal bumps on the electrodes on a semiconductor chip, the process comprising the steps of:

adhesive bonding low melting point metal balls each being spherically formed and having a given size to the respective electrodes, and

reflowing the low melting point metal balls.

The low melting point metal balls are preferably adhesive bonded to the respective electrodes with a flux. The flux is preferably applied to the electrodes.

Brief Description of the Drawings

Fig. 1 is a perspective view illustrating a semiconductor device of the present invention.

Fig. 2 is a view illustrating an electrode in the semiconductor device of the present invention.

Fig. 3 is a view illustrating a semispherical bump of the semiconductor device of the present invention which bump is formed by reflowing a low melting point metal ball.

Figs. 4A to 4D are views illustrating a process for producing the semiconductor device of the present invention.

Fig. 5 is a view illustrating a bump of a solder ball directly formed on a chip electrode of a single material.

Figs. 6A and 6B are views illustrating a preferred method for adhesive bonding low melting point metal balls to the respective electrodes.

Best Mode for Carrying Out the Invention

Fig. 1 shows a semiconductor device 1 of the present invention. The semiconductor device 1 is provided with low melting point metal ball bumps 3 adhesive bonded onto the electrodes (not shown) formed on a surface of a semiconductor chip 2.

The low melting metal balls 3 can be formed from one of the various solders used for mounting a semiconductor device on a substrate. Examples of the solders include solders of Sn alloys such as a Sn-Pb alloy and a Sn-Ag alloy and solders of Pb alloys such as a Pb-In alloy.

The electrodes to which the bumps 3 of low melting point metal balls are adhesive bonded can be formed from an electrode material of Cu or a Cu alloy, Al or an Al alloy, or Au or a Au alloy. In the semiconductor device of the present invention, an electrode having a surface area of 900 to 22,500 μm^2 is preferably used. That is, when a square electrode is used, one of the sides of the electrode has a dimension of 30 to 150 μm.

When the electrode material is Al or an Al alloy, connecting solder balls (the term solder balls designates low melting metal balls hereinafter and is used below) to an electrode by reflowing deteriorates the bonding between the solder balls and the electrode. When Al or an Al alloy is used as an electrode material, at least one layer of a metal or an alloy of the metal having a melting point higher than the electrode material is laminated to the layer formed of the electrode material to avoid the deterioration. A typical example of the material used as the material therefor is a metal selected from Ti, W, Ni, Cr, Au, Pd, Cu, Pt, Ag, Sn and Pb, or an alloy of these metals. Of these substances, Ti, W, Ni, Cr, Pd, Cu or Pt, or an alloy of these metals is particularly effective in bonding between the material and the layer formed from Al or its alloy. Accordingly, any of the above metals or an alloy of these metals is preferably used as a layer contacted with the layer of Al or its alloy. Moreover, a solder generally shows good wettability with Ni, Au, Pd, Cu, Pt, Ag, Sn or Pb, or an alloy of these metals. Of layers laminated to the electrode material layer of Al or an Al alloy, the layer contacted with the solder ball is, therefore, preferably formed from these materials.

As explained above, when Al or an Al alloy is used, the electrode has a multilayered structure as illustrated in Fig. 2. In Fig. 2, an electrode 8 is formed as a laminated structure including a first layer 5 made of Al (or an Al alloy) on a surface of a semiconductor chip 2, a

second layer 6 made of Cr on the first layer, and a third layer 7 made of Cu on the second layer.

In addition to the laminated structure successively having from the semiconductor chip side an Al (or Al alloy) layer, a Cr layer and a Cu layer (such a laminated structure being represented as Al/Cr/Cu hereinafter) as illustrated in Fig. 2, examples of the laminated structure of the electrode in which Al or its alloy is used as an electrode material may include Al/Ni, Al/Ni/Au, Al/Ni/Cu/Au, Al/Cr/Cu/Au, Al/Ti/Cu/Au, Al/Ti/TiW (alloy)/Cu/Au, Al/TiW (alloy)/Cu/Au, Al/Cr/Ni/Pd, Al/Pd/Au, Al/Ni/Sn, Al/Cr/Cu/Pd and Al/Cr/Pt. It is needless to say that effective electrode laminated structures are not limited to the structures mentioned above in the semiconductor device of the present invention.

A flux is preferably used for adhesive bonding the solder ball to the electrode. Any of the fluxes generally used in producing semiconductor devices may be used. Although the flux may be applied to either the solder ball or the electrode surface, it is preferably applied to the electrode surface. Standard methods such as screen printing may be utilized for the method for applying the flux to the electrode surface.

When the semiconductor device of the present invention is flip chip bonded to a substrate, the solder ball bumps may be made to face the respective electrode terminals of the substrate, positioned, and contacted therewith, followed by reflowing the bumps. Such a procedure of flip chip bonding has been widely known, and it is needless to explain in detail.

The semiconductor device of the present invention may be flip chip bonded to the substrate after the solder balls are reflowed once to form semispherical bumps. Fig. 3 shows an example of a semispherical bump. The semispherical bump 10 in Fig. 3 is formed by reflowing the

solder ball bump 3 adhesive bonded to the laminated electrode 8 having been explained in Fig. 2.

In addition, the bump 10 in Fig. 3 formed by reflowing a solder ball is herein described as semispherical. The term is mainly based on the longitudinal sectional shape of the bump subsequent to reflowing as shown in Fig. 3. Electrodes on semiconductor chips have various shapes such as a circular shape, a square shape and other arbitrary shapes. For example, a bump formed by reflowing a solder ball on a square electrode has a semispherical longitudinal sectional shape as seen in Fig. 3. However, since the molten solder wets the entire square electrode surface and then solidifies, the shape viewed from above (transverse sectional shape) is not a circle but a square or a shape close to a square. Accordingly, it should be noted that the semispherical bump herein termed includes not only a bump appearing to have a circular cross sectional shape when viewed from above after reflowing but also a bump having an arbitrary transverse cross sectional shape reflecting the electrode shape under the bump. That is, "a semispherical bump" herein designates all sorts of bumps formed by reflowing solder balls adhesive bonded to electrodes having an arbitrary shape.

In order to appropriately form a semispherical bump on an electrode by reflowing a solder ball, the radius R of the solder ball to be adhesive bonded to the electrode is desirably selected so that the equation

$$0.4\sqrt{A} \leq R \leq 2\sqrt{A}$$

wherein A is the surface area of the electrode, is satisfied. When the radius R of the solder ball is less than $0.4\sqrt{A}$, the amount of the solder becomes insufficient, and formation of a good semispherical bump subsequent to reflowing becomes difficult. When the radius R of the solder ball exceeds $2\sqrt{A}$, the semispherical bump becomes large compared with the size of the electrode. Consequently, the bonded portion between the electrode and

the bump is subjected to stress concentration, and tends to be fractured.

When an electrode having a surface area of 900 to 22,500 μm^2 is used in the semiconductor device of the present invention, a preferred radius R of the solder ball derived from the above equation is from 12 to 300 μm.

An example of the production of a semiconductor device in the present invention will be explained by making reference to Fig. 4.

As shown in Fig. 4A, a 100 x 100 μm electrode 42 1.0 μm thick of an Al alloy (Al-Si-Cu alloy) is formed on a semiconductor chip 41 by sputtering. The reference numeral 43 in the figure designates a passivation film which compartments the electrode thus formed. Next, a metal layer 44 of Ni and a metal layer 45 of Cu each having a thickness of 80 nm are successively laminated to the chip electrode 42 by sputtering, as shown in Fig. 4B.

What is explained above is about the step for forming a substrate on which a low melting point metal bump is to be formed. Next, as shown in Fig. 4C, a solder ball 46 of Pb-Sn alloy having a diameter of 80 μm is adhesive bonded to the Cu metal layer 45. At the time of adhesive bonding the solder ball, the surface of the metal layer 45 is first coated with a flux (not shown) by screen printing. In cases where, for example, the solder ball placed on the electrode is subsequently to be reflowed in a reducing atmosphere, coating the metal layer 45 with the flux may be omitted. The solder ball 46 is then adhesive bonded to the flux. A preferred method for adhesive bonding the solder ball to the electrode will be explained later.

The semiconductor device of the present invention thus prepared can be flip chip bonded to a substrate by making the solder ball bumps face the respective corresponding electrode terminals of the substrate, positioning the bumps, contacting the bumps with the respective electrode terminals thereof, and reflowing the bumps.

The semiconductor device of the present invention provided with the bumps of solder balls 46 as shown in Fig. 4C may also be flip chip bonded to the substrate after forming semispherical bumps 47 by reflowing the solder balls once as shown in Fig. 4D.

Since an Al alloy is used as an electrode material in the above example, the Ni layer and the Cu layer are laminated to the Al alloy layer so as to firmly bond the semiconductor device to the substrate by the solder bump. However, when the electrode material is neither Al nor Al alloy, for example, when the electrode material is Cu or a Cu alloy, or Au or a Au alloy, the substrate (one or more metal (or alloy) layers on the electrode material layer) for forming low melting point metal bumps is not required to be formed. Accordingly, as shown in Fig. 5, a bump of a solder ball 53 can be directly formed on an electrode 52 of a semiconductor chip 51. The solder ball bump may also be reflowed once to be formed into a semispherical bump, which is thereafter used for flip chip bonding.

Another example will now be described, in which solder ball bumps having a diameter of 150 μm are formed on an electrode having a diameter of 50 μm. In this case, Cr, Cu, and Au layers are successively superposed by sputtering process on an electrode of Al-Cu alloy having a diameter of 50 μm and a thickness of 1.0 μm, the superposed Cr, Cu, and Au layers having a thickness of 80 nm, 80 nm, and 30 nm, respectively, and a diameter which is the same as or somewhat larger than the diameter of the electrode. The surface of the Au layer is then coated with a flux, on which a solder ball of Pb-Sn alloy having a diameter of 150 μm is adhesive bonded. Shear test carried out for semispherical bumps formed by reflowing the solder balls revealed that all fractures occurred in the solder balls, and no fracture was observed at the bonded portions between the bumps and electrodes.

Next, a preferred method for adhesive bonding the solder balls to the electrodes will be explained. At

present, an explanation will be made of adhesive bonding the solder balls to not electrodes each having a multilayered structure but electrodes each composed of a single material as explained in Fig. 5.

As shown in Fig. 6A, a vibration at a small amplitude is applied to a vessel 60 containing the solder balls 53 to cause the solder balls 53 to jump up. The solder balls 53 are then arranged and held on an arrangement base plate 63 by attracting the jumping up solder balls 53 to attraction openings 61 (attracting mechanism for attracting the solder balls being not shown) provided in the arrangement base plate 63 in positions corresponding to positions of the electrodes of the semiconductor chip to which the solder balls 53 are to be adhesive bonded. During attracting and arranging the solder balls, excess solder balls 53' adhere to portions of the arrangement base plate 63 other than the attraction openings 61, or other excess solder balls 53" adhere to the solder balls 53 attracted to the attraction openings 61, as shown in Fig. 6A. The excess solder balls 53', 53" are, therefore, removed. To achieve the removal, arbitrary procedures may be utilized. For example, excess solder balls 53', 53" can be preferably removed by applying an ultrasonic vibration to the arrangement base plate 63 in the horizontal direction. Although only two attraction openings 61 are shown in the attraction base plate 63 in Fig. 6A for the sake of simplicity, it should be noted that the actual arrangement base plate has the attraction openings the number of which is the same as that of the solder balls to be adhesive bonded to the electrodes of the semiconductor chip.

Next, as shown in Fig. 6B, the arrangement base plate 63 holding the solder balls 53 in predetermined positions is moved above the semiconductor chip 51 so that the solder balls 53 are properly positioned with respect to the respective electrodes 52 of the semiconductor chip 51. The arrangement base plate 63 is then moved downward so

that the solder balls 53 are contacted with the respective electrodes 52. After the contact, attracting the solder balls 53 to the arrangement base plate 63 is stopped (by stopping the attraction mechanism), and the arrangement base plate 63 is moved upward.

When the surface of the electrodes 52 is coated with a flux (not shown in the figure), the solder balls 53 are adhesive bonded to the electrodes due to the adhesion thereof. When the surface of the electrodes 52 is not coated with a flux, semispherical bumps adhesive bonded to the respective electrodes 52 can be formed by, for example, reflowing the solder balls 53 in a reducing atmosphere, as referred to above.

Since solder bumps can simultaneously be adhesive bonded to a large number of the respective electrodes of a semiconductor chip by the process as explained above, the process is very advantageous to the production of the semiconductor device of the present invention.

In general, a large number of semiconductor chips are formed on one wafer, and separated by cutting to give individual chips. The process as mentioned above may also be applied to a plurality of semiconductor chips prior to separation of them from the wafer by cutting, or it may be applied to individual semiconductor chips subsequently to separation of them therefrom. It is evident from what has been explained above that the semiconductor chip in the present invention includes not only a separated individual semiconductor chip but also a plurality of semiconductor chips in a state of being produced on one wafer.

It is evident from what has been explained above that the semiconductor device of the present invention is provided with low melting point metal ball bumps directly adhesive bonded to the respective electrodes formed on a semiconductor chip. The bumps can be made of high quality by making the size of the metal balls uniform. The metal balls are not formed on the electrodes of the semiconductor chip by a procedure such as plating or vapor

deposition in conventional processes, but can be adhesive bonded to the electrodes. Accordingly, the semiconductor device of the present invention can be produced without a mask, and without fear of environmental pollution.

Furthermore, the amount of bumps can be easily and highly accurately controlled by adjusting the size of the low melting point metal balls, to enhance reliability of bumps.

Industrial Applicability

The present invention can be advantageously applied to flip chip bonding which makes possible high density mounting of a semiconductor device on a substrate.

CLAIMS

1. A semiconductor device comprising electrodes formed on a semiconductor chip, and bumps each consisting of a spherically formed low melting point metal ball having a given size, and adhesive bonded to the electrodes.

2. The semiconductor device according to claim 1, wherein the low melting metal balls are adhesive bonded to the electrodes with a flux.

3. The semiconductor device according to claim 1 or 2, wherein the electrodes are formed from an electrode material of Cu or a Cu alloy, Al or an Al alloy, or Au or a Au alloy.

4. The semiconductor device according to claim 3, wherein the electrodes each comprise a layer of an electrode material composed of Al or an Al alloy, and at least one metal layer or metal alloy layer laminated to the electrode material layer and having a melting point higher than the electrode material.

5. The semiconductor device according to claim 4, wherein the at least one layer laminated to the electrode material layer is formed from a metal selected from Ti, W, Ni, Cr, Au, Pd, Cu, Pt, Ag, Sn or Pb or an alloy of these metals.

6. The semiconductor device according to claim 5, wherein the at least one layer laminated to the electrode material and contacted with the electrode material layer is formed from Ti, W, Ni, Cr, Pd, Cu or Pt, or an alloy of these metals, and the at least one layer farthest from the electrode material layer contacted with the low melting point metal ball is formed from Ni, Au, Pd, Cu, Pt, Ag, Sn or Pb, or an alloy of these metals.

7. A process for producing a semiconductor device comprising electrodes formed on a semiconductor chip, and bumps each consisting of a low melting point metal ball spherically formed, having a given size and adhesive bonded to the electrodes, the process comprising adhesive

bonding the low melting point metal balls to the electrodes with a flux.

8. The process according to claim 7, wherein the flux is applied to the electrodes.

9. The process according to claim 7 or 8, wherein the low melting point metal balls are adhesive bonded to the electrodes by a process comprising the steps of:

applying a vibration at a small amplitude to a vessel containing the low melting point metal balls to cause the low melting point metal balls to jump up;

arranging and holding the low melting point metal balls on an arrangement base plate by attracting the jumping up low melting point metal balls to attraction openings provided in the arrangement base plate in positions corresponding to the electrodes of the semiconductor chip to which the low melting point metal balls are to be adhesive bonded;

removing excess low melting point metal balls adhering either to the arrangement base plate or to the low melting point metal balls attracted to the attraction openings; and

simultaneously contacting the low melting point metal balls held and arranged on the arrangement base plate with the electrodes of the semiconductor chip.

10. A process for producing a semiconductor device provided with low melting point metal bumps on a semiconductor chip, the process comprising the steps of:

adhesive bonding low melting point metal balls each being spherically formed and having a given size to the electrodes, and

reflowing the low melting point metal balls.

11. The process according to claim 10, wherein the low melting point metal balls are adhesive bonded to the respective electrodes with a flux.

12. The process according to claim 11, wherein the flux is applied to the electrodes.

13. The process according to any one of claims 10 to 12, wherein the low melting point metal balls are adhesive bonded to the electrodes by a process comprising the steps of:

applying a vibration at a small amplitude to a vessel containing the low melting point metal balls to cause the low melting point metal balls to jump up;

arranging and holding the low melting point metal balls on an arrangement base plate by attracting the jumping up low melting point metal balls to attraction openings provided in the arrangement base plate in positions corresponding to the electrodes of the semiconductor chip to which the low melting point metal balls are to be adhesive bonded;

removing excess low melting point metal balls adhering either to the arrangement base plate or to the low melting point metal balls attracted to the attraction openings; and

simultaneously contacting the low melting point metal balls held and arranged on the arrangement base plate with the electrodes of the semiconductor chip.

14. A semiconductor device produced by the process according to any one of claims 7 to 9, and provided with bumps consisting of low melting point metal balls and adhesive bonded to the respective electrodes of a semiconductor chip.

15. A semiconductor device produced by the process according to any one of claims 10 to 13, and provided with bumps consisting of low melting point metal on the electrodes of a semiconductor chip.

Fig.1

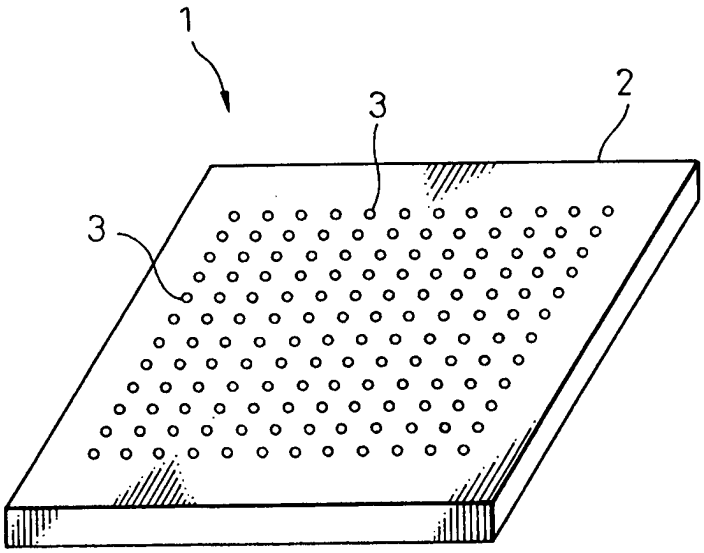


Fig. 2

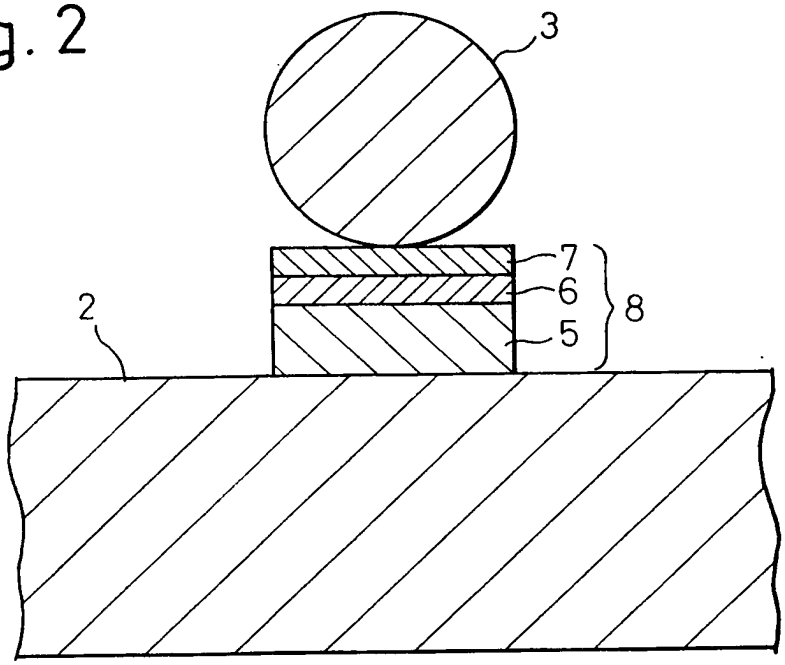


Fig. 3

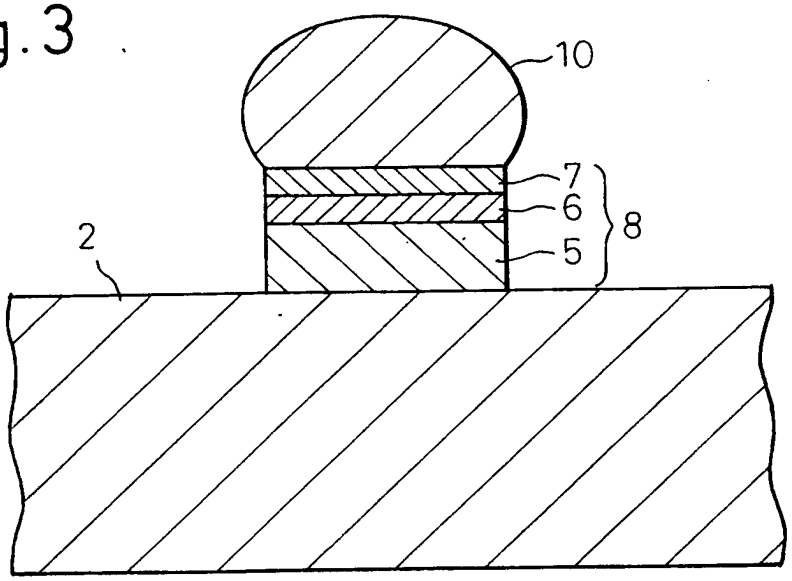


Fig. 4A

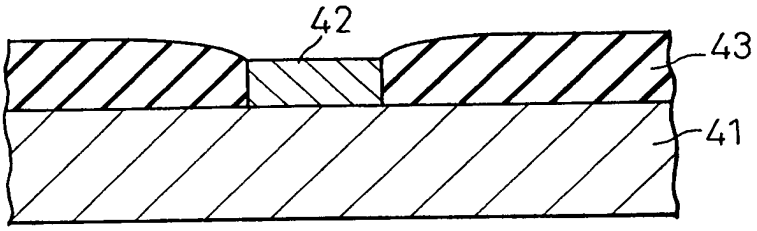


Fig. 4B

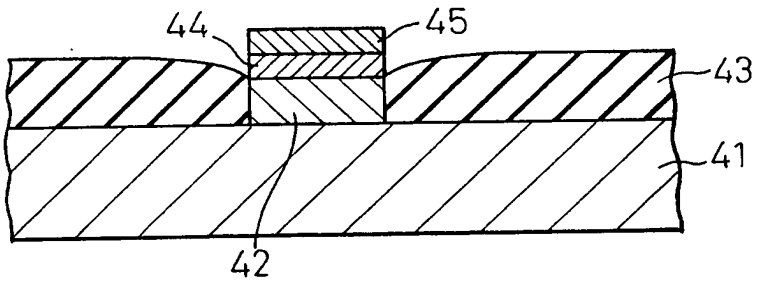


Fig. 4C

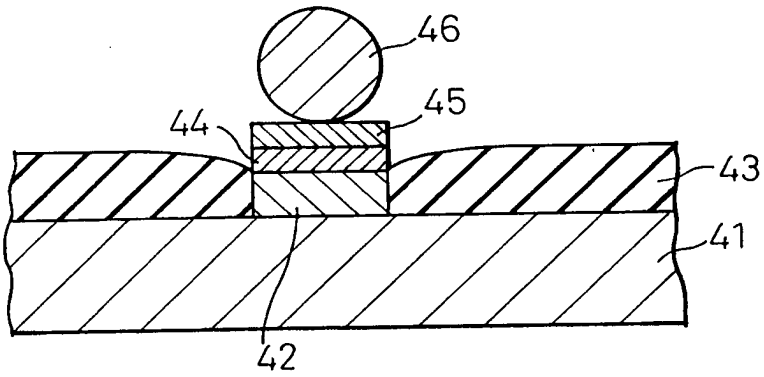


Fig. 4D

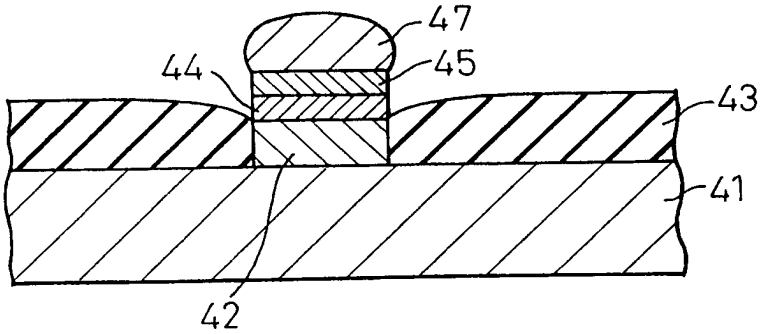


Fig.5

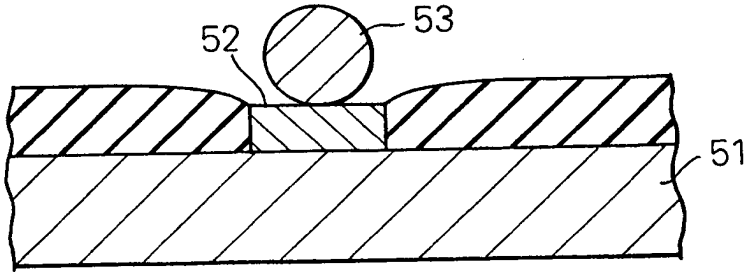


Fig.6A

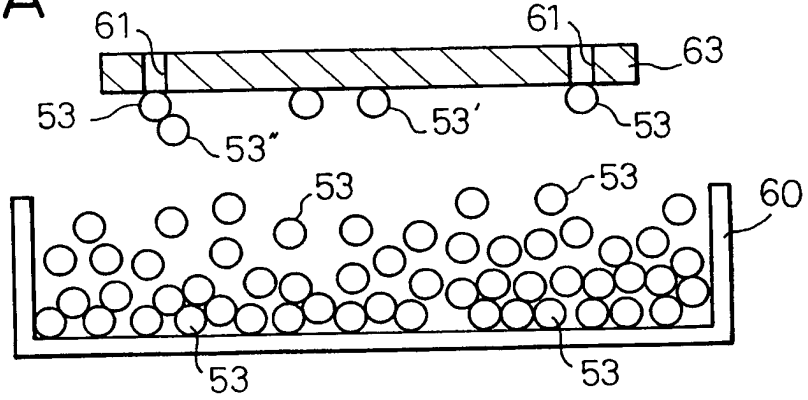
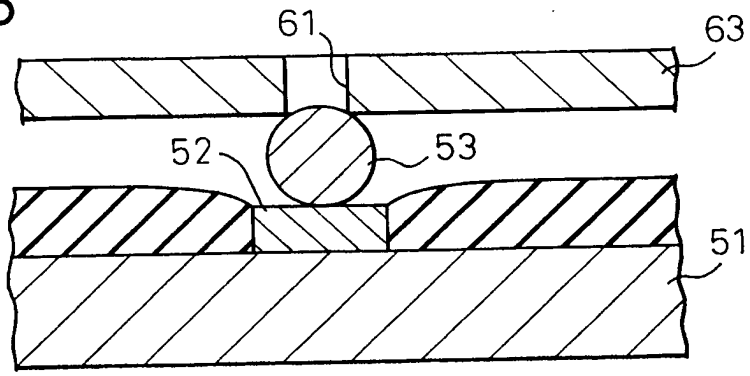


Fig.6B



INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 97/02987

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/485

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimumdocumentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	PATENT ABSTRACTS OF JAPAN vol. 097, no. 007, 31 July 1997 & JP 09 082719 A (NIPPON STEEL CORP), 28 March 1997, see the whole document ---	1,2,7,8, 10-12, 14,15
X	PATENT ABSTRACTS OF JAPAN vol. 095, no. 003, 28 April 1995 & JP 06 333930 A (OKI ELECTRIC IND CO LTD), 2 December 1994, see the whole document ---	1,2,7,8, 10-12, 14,15
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 082 (E-1038), 26 February 1991 & JP 02 299288 A (FUJITSU LTD), 11 December 1990, see the whole document ---	1,2,7,8, 10,11, 14,15
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of theinternational search	Date of mailing of the international search report
12 January 1998	23/01/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Zeisler, P

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 97/02987

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X Y	PATENT ABSTRACTS OF JAPAN vol. 096, no. 009, 30 September 1996 & JP 08 118005 A (MATSUSHITA ELECTRIC IND CO LTD), 14 May 1996, see the whole document & US 5 655 704 A (MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.) 12 August 1997 see column 6, line 16 - line 43; figure 4	1,2,7,8, 10,11, 14,15 9,13
A	PATENT ABSTRACTS OF JAPAN vol. 008, no. 281 (E-286), 21 December 1984 & JP 59 148352 A (SEIKO DENSHI KOGYO KK), 25 August 1984, see the whole document	1-7,10, 11
A	US 5 219 117 A (LIN PAUL T) 15 June 1993 see the whole document	1,3-7, 10,14,15
Y	EP 0 527 387 A (NIPPON STEEL CORP) 17 February 1993 see column 9, line 38 - column 10, line 4; figures 3A,3B	9,13
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 275 (E-1219), 19 June 1992 & JP 04 065130 A (FUJITSU LTD), 2 March 1992, see abstract	9,13
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 046 (E-1029), 4 February 1991 & JP 02 278831 A (FUJITSU LTD), 15 November 1990, see abstract	9,13

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 97/02987

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5219117 A	15-06-93	NONE	
EP 0527387 A	17-02-93	JP 3097237 A	23-04-91
		JP 3097240 A	23-04-91
		DE 69027448 D	18-07-96
		DE 69027448 T	10-10-96
		EP 0427384 A	15-05-91
		KR 9404246 B	19-05-94
		US 5164336 A	17-11-92
		US 5114878 A	19-05-92
		JP 1995827 C	08-12-95
		JP 3174737 A	29-07-91
		JP 7019800 B	06-03-95

·6

PATENT COOPERATION TREATY

REC'D 26 NOV 1998
WIPO PCT

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference E876-PCT	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (PCT/IPEA/416)
International application No. PCT/JP97/02987	International filing date *(day/month/year)* 27/08/1997	Priority date *(day/month/year)* 27/08/1996
International Patent Classification (IPC) or national classification and IPC H01L23/485		
Applicant NIPPON STEEL CORPORATION et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of sheets.

3. This report contains indications relating to the following items:

I	☒	Basis of the report
II	☐	Priority
III	☐	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
IV	☐	Lack of unity of invention
V	☒	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
VI	☒	Certain documents cited
VII	☒	Certain defects in the international application
VIII	☒	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
27/03/1998	25.11.98
Name and mailing address of the IPEA/ European Patent Office D-80298 Munich Tel. (+49-89) 2399-0, Tx: 523656 epmu d Fax: (+49-89) 2399-4465	Authorized officer Cousins, D Telephone No. (+49-89) 2399-2759

Form PCT/IPEA/409 (Cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/JP97/02987

I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-12 as originally filed

Claims, No.:

1-15 as originally filed

Drawings, sheets:

1/4-4/4 as originally filed

2. The amendments have resulted in the cancellation of:

☐ the description, pages:
☐ the claims, Nos.:
☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	3-6, 9, 13
	No:	Claims	1, 2, 7, 8, 10-12, 14, 15
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-15
Industrial applicability (IA)	Yes:	Claims	1-15
	No:	Claims	

2. Citations and explanations

see separate sheet

VI. Certain documents cited

1. Certain published documents (Rule 70.10)

and / or

2. Non-written disclosures (Rule 70.9)

see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Section V

1. Reference is made to the following documents:

D1: PATENT ABSTRACTS OF JAPAN vol. 095, no. 003, 28 April 1995; & JP 06 333930 A (OKI ELECTRIC IND CO LTD), 2 December 1994.
D2: PATENT ABSTRACTS OF JAPAN vol. 008, no. 281 (E-286), 21 December 1984 & JP 59 148352 A (SEIKO DENSHI KOGYO KK), 25 August 1984*.
D3: PATENT ABSTRACTS OF JAPAN vol. 015, no. 046 (E-1029), 4 February 1991; & JP 02 278831 A (FUJITSU LTD), 15 November 1990*.
D4: PATENT ABSTRACTS OF JAPAN vol. 015, no. 082 (E-1038), 26 February 1991; & JP 02 299288 A (FUJITSU LTD), 11 December 1990.
D5: PATENT ABSTRACTS OF JAPAN vol. 096, no. 009, 30 September 1996; & JP 08 118005 A (MATSUSHITA ELECTRIC IND CO LTD), 14 May 1996.
D6: PATENT ABSTRACTS OF JAPAN vol. 097, no. 007, 31 July 1997; & JP 09 082719 A (NIPPON STEEL CORP), 28 March 1997.

*Copies of the JP-A documents are annexed.

2. The present application does not meet the requirements of Article 33(2) PCT, because, insofar as it is clear (see Section VIII), the subject-matter of claims 1, 2, 7, 8, 10-12, 14 and 15 is not new.

2.1 The semiconductor device, and method for manufacture thereof, known from D1 comprises electrodes (2) formed on a semiconductor chip (1), and bumps (6) each consisting of a spherically formed low melting point metal ball having a given size and being adhesively bonded to the electrodes via flux (7), the latter being applied to the electrodes (**re. claims 1, 2, 7, 8, 14**).

It can be assumed that the solder balls (6) in the known method are subjected to a reflow process (**re. claims 10-12, 15**).

3. Dependent **claims 3-6, 9 and 13** comprise features which are not found in combination in any single prior art document such that these claims comprise subject-matter which is novel (Article 33(2) PCT), however these claims do not

contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step (Article 33(3) PCT), the reasons being as follows:

3.1 A semiconductor element is known from D2 having an Al wiring (3) formed on the surface thereof and exposed as a wiring terminal part; a Cu film (5) is formed on the exposed part of the Al wiring (3) and a Cu film is formed as the barrier layer (6). A solder ball (8) is applied to the barrier layer (6). According to the JP-A document (see page 244, references to the figures 1, 2), it appears that the initial metal layer on the Al wiring layer may be Cr.
Therefore the additional features of dependent **claims 3-6** are known from D2; it would be a matter of routine for the skilled person to use the metals known from D2 in the semiconductor device known from D1.

3.2 The process for applying the low melting point metal balls to an electrode on an insulating substrate for a semiconductor device known from D3 has the steps of:
levitating the metal balls (4) from a vessel containing them;
arranging and holding the metal balls on a base plate (11, 17), the latter having openings (11a, 17a) in positions corresponding to the electrodes (2) of the insulating substrate to which the metal balls (4) are to be bonded;
removing excess metal balls (inherent in D3);
contacting the metal balls with the electrodes of the insulating substrate.

Consequently the subject matter of dependent **claims 9 and 13** is obvious to the skilled person starting from D3 and realising that bumps can be formed on a semiconductor chip by the method of D3, the additional step of applying a flux to the electrode per se being normal in the art, see D1, D4, or D5.

4. Although it relates to a circuit board, not to a semiconductor chip, document D4 anticipates claims 1, 2, 7, 8, 10-12, 14 and 15. Document D5 is novelty destroying for claims 1, 2, 7, 8, 10, 11, 14 and 15, it being clear that there is a layer of flux provide between the electrode (2a) and the solder ball (3), see lower figure of abstract.

Section VI

Notwithstanding that the priority of the following document and of the present application have not been checked, a copy of the latter not being available to the IPEA, the document D6 appears to be relevant for the purposes of novelty in respect of claims 1, 2, 7, 8, 10-12, 14 and 15.

Section VII

1. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1-D5 is not mentioned in the description, nor are these documents identified therein.

2. The independent claims are not in the two-part form in accordance with Rule 6.3(b) PCT, which in the present case would be appropriate, with those features known in combination from the prior art being placed in a preamble (Rule 6.3(b)(i) PCT) and with the remaining features being included in a characterising part (Rule 6.3(b)(ii) PCT).

Section VIII

1. The various definitions of the invention given in independent claims 7 and 10 are such that the claims as a whole are not concise, contrary to Article 84 EPC. The plurality of independent claims makes it difficult, if not impossible, to determine the matter for which protection is sought, and places an undue burden on others seeking to establish the extent of the protection. The claims should be recast to include only the minimum necessary number of independent claims in any one category, Rule 29(2) EPC, with dependent claims as appropriate, Rule 29(4) EPC.

2. The term "spherically formed" in claim 1 may raise doubt as to whether this should mean that the ball is spherical in the final product or whether this is reference to a method step; the final ball does not appear to be spherical in Figures 3 and 4.

3. Claims 14 and 15 are unclear since they are formulated as a product-by-process.

Claims directed to products defined by their method of manufacture are only allowable if the products as such fulfill the requirements for patentability and the application contains no other disclosure that could enable the applicant to adequately define the product by virtue of its composition, structure or some other testable parameter (cf Headnote II, T 150/82, OJ EPO, 1984, 309). The products as such must, for patentability to be acknowledged, be in themselves new and inventive. The definitive in terms of the method step is not considered to be restrictive.

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

United States Patent and Trademark Office
(Box PCT)
Crystal Plaza 2
Washington, DC 20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 27 April 1998 (27.04.98)	
International application No. PCT/JP97/02987	**Applicant's or agent's file reference** E876-PCT
International filing date (day/month/year) 27 August 1997 (27.08.97)	**Priority date** (day/month/year) 27 August 1996 (27.08.96)
Applicant TATSUMI, Kohei et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

27 March 1998 (27.03.98)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer K. Takeda
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 97/02987

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/485

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	PATENT ABSTRACTS OF JAPAN vol. 097, no. 007, 31 July 1997 & JP 09 082719 A (NIPPON STEEL CORP), 28 March 1997, see the whole document ---	1,2,7,8, 10-12, 14,15
X	PATENT ABSTRACTS OF JAPAN vol. 095, no. 003, 28 April 1995 & JP 06 333930 A (OKI ELECTRIC IND CO LTD), 2 December 1994, see the whole document ---	1,2,7,8, 10-12, 14,15
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 082 (E-1038), 26 February 1991 & JP 02 299288 A (FUJITSU LTD), 11 December 1990, see the whole document ---	1,2,7,8, 10,11, 14,15

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 January 1998	23/01/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040 Tx. 31 651 epo nl	

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 97/02987

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	PATENT ABSTRACTS OF JAPAN vol. 096, no. 009, 30 September 1996 & JP 08 118005 A (MATSUSHITA ELECTRIC IND CO LTD), 14 May 1996, see the whole document & US 5 655 704 A (MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.) 12 August 1997 see column 6, line 16 - line 43; figure 4	1,2,7,8, 10,11, 14,15 9,13
A	PATENT ABSTRACTS OF JAPAN vol. 008, no. 281 (E-286), 21 December 1984 & JP 59 148352 A (SEIKO DENSHI KOGYO KK), 25 August 1984, see the whole document	1-7,10, 11
A	US 5 219 117 A (LIN PAUL T) 15 June 1993 see the whole document	1,3-7, 10,14,15
Y	EP 0 527 387 A (NIPPON STEEL CORP) 17 February 1993 see column 9, line 38 - column 10, line 4; figures 3A,3B	9,13
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 275 (E-1219), 19 June 1992 & JP 04 065130 A (FUJITSU LTD), 2 March 1992, see abstract	9,13
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 046 (E-1029), 4 February 1991 & JP 02 278831 A (FUJITSU LTD), 15 November 1990, see abstract	9,13

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 97/02987

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5219117 A	15-06-93	NONE	
EP 0527387 A	17-02-93	JP 3097237 A	23-04-91
		JP 3097240 A	23-04-91
		DE 69027448 D	18-07-96
		DE 69027448 T	10-10-96
		EP 0427384 A	15-05-91
		KR 9404246 B	19-05-94
		US 5164336 A	17-11-92
		US 5114878 A	19-05-92
		JP 1995827 C	08-12-95
		JP 3174737 A	29-07-91
		JP 7019800 B	06-03-95